

LIST OF PUBLICATIONS FOR  
APPLICANT'S INFORMATION  
DISCLOSURE STATEMENT

Applicant: Berenbaum et al.  
Case: 7-2-3-3  
Serial No.: 09/538,670  
Filing Date: March 30, 2000  
Group: 2154

## U.S. PATENT DOCUMENTS

EXAMINER	DOCUMENT NO.	DATE	NAME	CLASS/SUBCLASS	FILING DATE
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EXAMINER	DOCUMENT NO.	DATE	COUNTRY	CLASS/SUBCLASS	TRANSLATION YES NO
<i>[Signature]</i>	EP 0 827 071 A2	03/04/98	<i>[Signature]</i> Europe		RECEIVED JUN 11 2003

## OTHER DOCUMENTS

EXAMINER	REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.	Technology Center 2100
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*[Signature]* Berkerman et al., "Performance and Hardware Complexity Tradeoffs in Designing Multithreaded Architectures," IEEE Proceedings of PACT, pgs. 24-34 (1996).  
*[Signature]* Hirata et al., "An Elementary Processor Architecture with Simultaneous Instruction Issuing from Multiple Threads," Computer Architecture News, Association for Computing Machinery, vol. 20, no. 2, pgs. 136-145 (1992).  
*[Signature]* Mombers et al., "A Multithreaded Multimedia Processor Merging On-Chip Multiprocessors and Distributed Vector Pipelines," Proceedings of IEEE Inter'l Symposium on Orlando, Florida, pgs 287-290 (1999).

Examiner: *[Signature]*Date Considered: *11/08/04*

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609, draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.